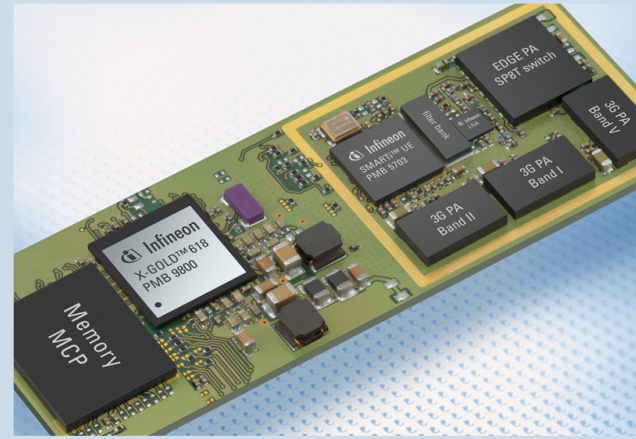


MIPI HSI IP

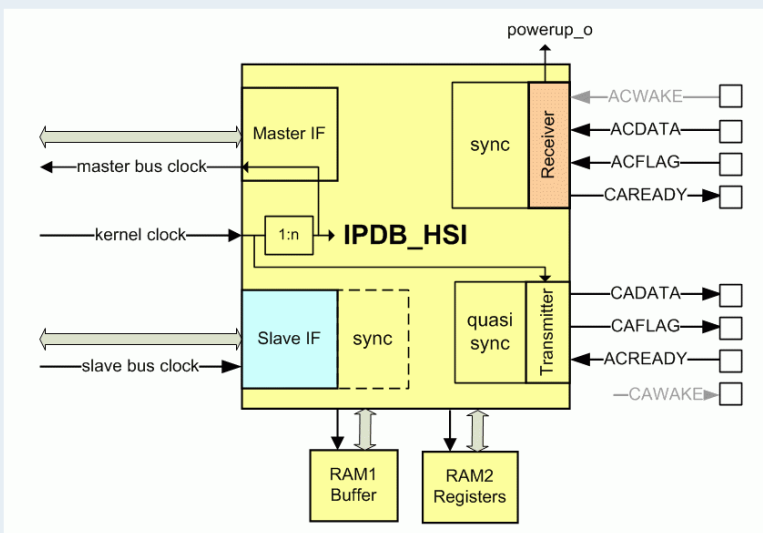
High-Speed Synchronous Serial Interface Physical Layer IP



Introduction

The HSI is a Mobile Industry Processor Interface (MIPI) Alliance standard. It can be used to connect a cellular modem chip to an application processor.

The serial protocol uses the signals DATA and FLAG as combined data and clock signals. The signal READY is used for flow control purposes. An optional WAKE signal is used to wakup the chip from standby.



Standard Compliance

- MIPI HSI Physical Layer Version 1.01
- AHB 2.0

MIPI HSI Features

- Serial Interface
- 16 RX + 16 TX channels
- Flow controlled
- Standby support
- Run time configurable
- Error detection

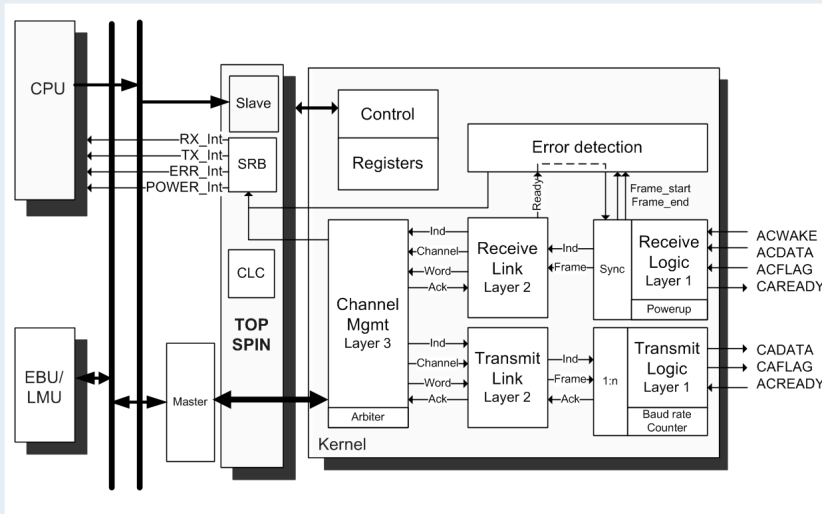
IP Features

- Self clocked input circuit
- System powerup support
- Channel management
- Priority channel support
- Direct memory access
- Single/double or ringbuffer access
- Interrupt support

MIPI HSI IP

Description

The DICE IP softcore represents a complete peripheral device with master and slave interfaces to the system bus. Provided interfaces are AHB 2.0 for both master and slave or alternatively AXI 3.0 master interface. Customized bus interfaces are available on request.



The processor configures the peripheral over the slave interface. Received data is written to system memory by the master interface. Data to transmit is read from system memory by the master interface. The processor is informed by interrupts about data reception and transmission status.

The data is organized in configurable channel buffers in system memory. These buffers can be used as single, double or ring buffers.

The error detection recognizes timeouts and unexpected bits. It stops reception in case of errors and informs the processor by interrupt to handle the error.

The system can be woken up by the input signal ACWAKE or a change on the lines ACFLAG/ACDATA.

System Bus Interfaces

- AHB 2.0 slave interface
- AHB 2.0 or AXI 3.0 master interface
- Customized interface on request

Benefits

- Easy integration as RTL softcore
- Low processor load
- Power-optimized design
- Scan insertion ready design
- Reuseable Verification on Toplevel
- Standard conform (MIPI contributor)

Deliverables

- Synthesizable VHDL RTL source code
- Specman® Verification environment
- Synopsys TCL scripts for synthesis and scan insertion
- Architecture and integration specification

Contact

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